

IET Computers and Digital Techniques Call for Papers

SPECIAL ISSUE ON: Asynchronous Circuits and Systems

A considerable shift is taking place in semiconductor design and architecture. This transformation is occurring due to two major factors. First, power has replaced performance as the most critical design metric, whether the design is for hand held devices or high performance processing. Second, the exponential increase in the number of transistors on a chip has grown to the point that a single clock frequency for all components over constrains the design. Thus modern design contains multiple frequency domains highly optimized for power. This transformation has created new potential for asynchronous circuit technology that enables modular low power design. Scaling now highlights the significant need for design and validation methodologies, techniques, and tools for asynchronous systems.

IET Computers and Digital Techniques seeks original manuscripts for a special issue on asynchronous circuits and systems, scheduled for publication in April 2011. This special issue aims at introducing readers to the state of the art in asynchronous design methodology and tools.

- asynchronous/mixed-timed circuits, architectures, memories and interfaces, including interfaces with analogue and mixed-signal domains
- asynchronous power-adaptive computing, ultra-low power systems, electronics for energy harvesting
- asynchrony in emerging technologies, including genetic, neural, nano and quantum computing
- embedded system design with asynchronous architectures and implementations
- elastic and latency-tolerant synchronous design and GALS systems
- formal methods for correctness, and performance/power analysis
- design models and methods for asynchronous buses, Networks-on-Chip (NoC), System-on-Chip (SoC) and multi-chip interconnects
- synchronization, arbitration, metastability modelling and analysis
- CAD tools for asynchronous design, synthesis, analysis and optimization
- physical design of asynchronous logic and pipelines
- test, reliability, security, and radiation tolerance
- motivating case studies, comparisons, and applications
- asynchronous variability-tolerant design and design for manufacturing

All papers must be submitted through the journal's Manuscript Central system:
<http://mc.manuscriptcentral.com/iet-cdt>

Proposed publication schedule:

Deadline for submission of papers: 1 August 2010

Authors to receive a 1st decision by:

15 October 2010

Final notification of acceptance:

1 January 2011

On-line and print publication:

Q2 2011

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